Digital Current Mode Control for Buck-Converter Based on Average Inductor Current Measurement

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***Abstract*— This paper introduces a digitally performed current mode and voltage control for the dc-dc step down converter based on voltage to frequency converter where the average values of inductor current and output voltage are obtained. These current and voltage measurement are realized by the voltage control oscillator (VCO) and counters (digital integrator). Such an approach enables full digitalization of current and voltage control loops.**

Keywords—DC-DC converters, converter control, current control

I. INTRODUCTION

Digitally controlled pulse-width modulation (PWM) converters have many potential advantages, including programmability, insensitivity to parameter variations, reduction of external passive components, as well as the potential to apply more advanced algorithms for the control and protection. When using microprocessors the computing capabilities are not fast enough to calculate the necessary time critical calculations for the control algorithm during the switch period. Later, advances in digital technology prompted some research groups to use Field-Programmable Gate Array's (FPGA's) or Digital Signal Processors (DSP's) [1], [2] and [3]. In the current mode, the switch or the inductor current is sensed within an inner loop and replaces the conventional saw-tooth waveform when generating the Pulse Width Modulation (PWM) function. Such algorithms were used within the domain of the analogue solution but recently, some algorithms were mainly developed based on an instantaneous current measurement and prediction strategy [4], [5].

According to digital approach in order to solve DC-DC converter control function it must be noted that the digital controller samples the sensed current at least twice in switching period and the actual trajectory of the inductor current is unknown to the controller. According to digital control approach the current must be sampled at least twice during the switching period in order to solve DC-DC converter control function whereas the actual trajectory of the inductor current is is unknown to the controller. Some research work was done in digitalization area where prediction method was used. The inductor current has been sampled at least twice, when the current was rising (within T_{on} interval) or falling (within T_{off} interval) as was discussed in [4]. By using such algorithm the peak or valley current-mode control could be applied.

This paper explores a current mode control for a dc-dc buck converter based on the average value of the inductor current measurement, by using a voltage-controlled oscillator

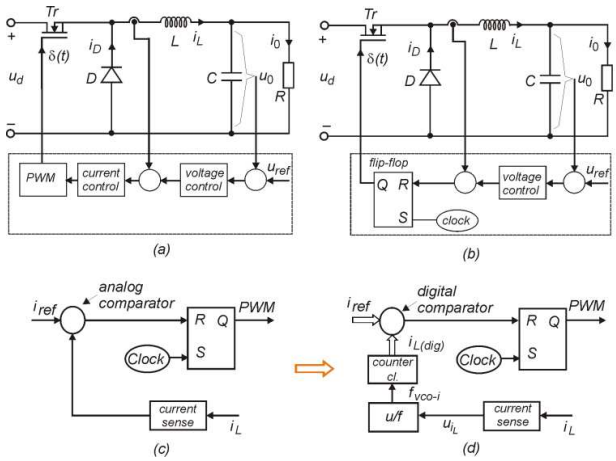

Figure 1. (a) The buck converter schema - analog architecture; (b) The buck converter schema - current-mode analog architecture; (c) current modulator-analog solution; (d) current-modulator, digital solution

and digital counter for the inductor current measurement. The algorithm was investigated theoretically and verified by simulation and experimentation.

II. PRINCIPLE OF OPERATION

The block diagram of a cascade controlled buck converter and analog current mode control schema is shown in Fig. 1 (a) and (b) respectively. The current reference i_{ref} is obtained as an output of the voltage controller. Better dynamics response can be achieved by the use of current-mode control schema. The conventional PI controller and the saw-tooth waveform generator (Fig. 1 (a)) which is used to generate the PWM signal is replaced with the inner current loop. Replacement of the inner current loop Fig. 1 (b) is done by the introduction of the switch (i_{sw}) or inductor current (i_L) which is compared to the current reference signal. The resulting signal is led to the R-S flip-flop in order to generate the triggering pulse for the transistor (PWM signal). For the digital implementation the structure of Fig. 1 (b) cannot be directly used. The digitalization principles, which will be considered here, enable and/or provide the current information also during the sampling interval. The new digital principle of current

- mode control is proposed in Fig. 1 (d). Voltage-controlled oscillators (VCO) and digital counters were used instead of classical A/D converters. VCO is also known as voltage-frequency converters (u/f converter). Such organized control of the buck converter is shown in Fig. 2.

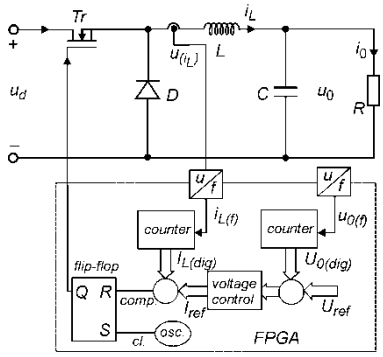

Figure 2. Current mode concept:(a) Ordinary PWM approach; (b) Current-mode control replacing the classical PWM..

A. The current-mode control operation

Referring to Fig 2, in steady state the current control function is started when the clock pulse (*cl* .) appears. For the sake of simplicity in the block schema only one counter is shown, but the actual signal (from u/f) is divided into two clock signals $i_{L(f\text{-}on)}$ and $i_{L(f\text{-}off)}$ for the two counters indicated in signal diagrams in Fig. 3. Both signals are led to the appropriate counters. Comparator resets the flip-flop if the sum of both counters contents meet reference current i_{ref}, represented by 16-bit digital numbers. The counter "integrates" the VCO pulses $i_{L(f\text{-}off)}$ during the T_{off} interval simply by counting and as an output the $I_{L(dig)}$ signal is generated.

B. Current-measurement mathematical analysis

The instantaneous VCO frequency of these pulses (f_i) can be calculated from:

$$f_i = k u_{iL}(t) + f_0 \tag{1}$$

where f_0 represents offset frequency, and k is the VCO constant (for chosen VCO, f_0=23 MHz and $k = 15.6$ MHz/V). Voltage u_{iL} appears on the VCO input after the inductor current was measured at the shunt resistor (R_{sh}) and amplified with the (A_β) constant. It yields

$$u_{iL} = A_\beta R_{sh} i_L \tag{2}$$

where

$$i_L(t) = \begin{cases} i_{\max} - a_1 t; & \text{when } Tr = OFF \\ i_{\min} + a_2 t; & \text{when } Tr = ON \end{cases} \tag{3}$$

The current has a maximum indicated by i_{max} and minimum indicated by i_{min} (Fig. 3). Coefficients a_1 and a_2 depend on the circuit parameters (u_d - u_o)/L and -u_o/L respectively.

The new clock signal appears at the end of interval T_{off} where the flip-flop is set and the *Tr* is switched ON. At the same time another counter also starts, which integrates the pulses of VCO

during the interval T_{on}. The reset signal appears on the *R* flip-flop input when the sum of both counters reach reference current, and *Tr* is switched OFF.

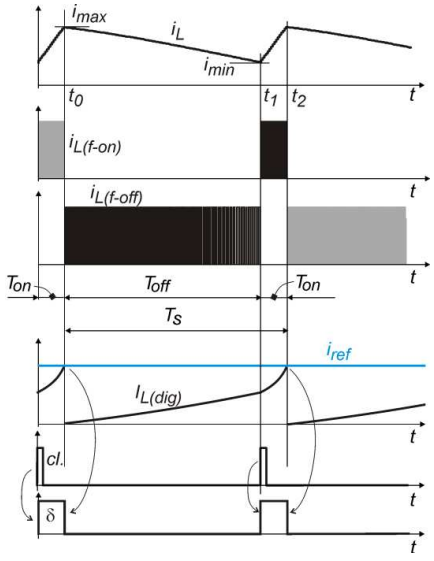

Figure 3. The typical waveforms: i_L-inductor current; $i_{L(f\text{-}on)}$-VCO signal for inductor current when *Tr* is ON, $i_{L(f\text{-}off)}$-VCO signal for inductor current when *Tr* is OFF, $I_{L(dig)}$-contets of counter (average inductor current); *cl*-flip- flop clock signal; δ– PWM-triggering pulse.

Both counters must be reset to zero in order to start the new current measurement. This procedure is repeated during the converter operation. The VCO generates an output signal $i_{L(f\text{-}on)}$ connected as a clock signal to the digital counter. The same VCO output signal is connected inside the FPGA on the two counters. VCO frequency $\left(f_{i-off}\right)$ changes during interval T_{off} as follows from (1), (2) and (3):

$$f_{i-off} = \Lambda_1 - \Lambda_2 t \tag{4}$$

where $\Lambda_1 = kA_\beta R_{sh} i_{\max} + f_0$ and $\Lambda_2 = kA_\beta R_{sh} a_1$ and also VCO frequency changes during T_{on}:

$$f_{i-on} = \Gamma_1 + \Gamma_2 t \tag{5}$$

where $\Gamma_1 = kA_\beta R_{sh} i_{\min} + f_0$ and $\Gamma_2 = kA_\beta R_{sh} a_2$. Equations (4) and (5) show how the instantaneous value of inductor current changes the VCO frequency. In order to evaluate the inductor current average value next formula must be used:

$$\begin{aligned} I_L &= \frac{1}{T_s}\int_{t_0}^{t_2} i_L(t)\,dt = \frac{1}{T_s}\int_{t_0}^{t_2} K_1 f_i(t)\,dt \\ &= \frac{K_1}{T_s}\left(\int_{t_0}^{t_1} f_{i-off}(t)\,dt + \int_{t_1}^{t_2} f_{i-on}(t)\,dt\right) \end{aligned} \tag{6}$$

where K_1 is digital scaling factor. Equation (6) is modified by using notations in Fig. (4) as follows:

$$\frac{I_L T_s}{K_1} = \int_0^x f_{i-off}(\tau)d\tau + \int_0^y f_{i-on}(\tau)d\tau = \Lambda_1 x - \Lambda_2 \frac{x^2}{2} + \Gamma_1 y + \Gamma_2 \frac{y^2}{2} \quad (7)$$

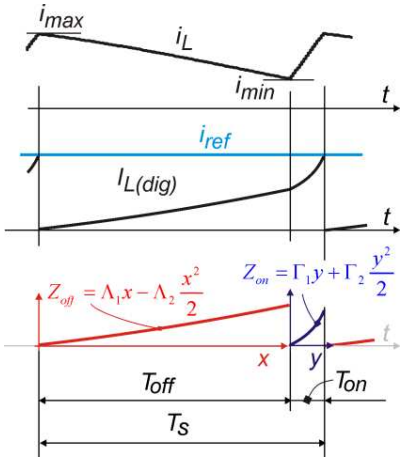

Figure 4. The waveforms: inside measurement circuit.

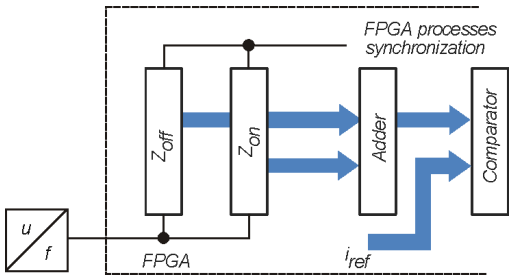

Figure 5. Conceptual scheme of inductor current measurement.

So at the end of integration process (end of interval T_s) inside of FPGA the average value of the inductor current is available as the state of adder (refer Fig. 5).

$$\frac{I_L T_s}{K_1} = Z_{off} + Z_{on} = Z_{(iL)} \quad (8)$$

where

$$Z_{off} = \Lambda_1 x - \Lambda_2 \left(x^2/2\right) \text{ and } Z_{on} = \Gamma_1 y + \Gamma_2 \left(y^2/2\right).$$

From (8) it can be evaluated the inductor current average value over the interval T_s, as follows

$$I_L = Z_{(iL)} \frac{K_1}{T_s} \quad (9)$$

C. Voltage-measurement mathematical analysis

Referring to Fig 2, in steady state the voltage control function is started when the clock pulse (*cl* .) appears. The VCO converts voltage into frequency:

$$f_u = a_t u_0(t) + f_0 \quad (10)$$

Where a_t is the measurement resistor attenuation, f_0 is the VCO offset frequency and voltage $u_0(t)$ is represents by:

$$u_0(t) = U_0 \quad (11)$$

The VCO is started with voltage to frequency conversion and generates at its output pulses indicated as $u_{0(f)}$ in Fig. 6. At the same time this VCO signal is counted by counter and at the end of T_s interval there is an "average" output voltage available as follows:

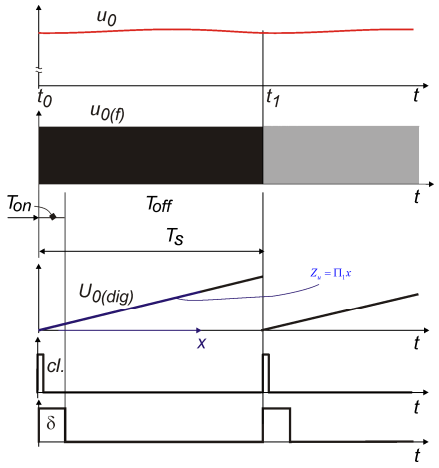

Figure 6. The voltage measurement waveforms: u_0-output voltage; $u_{0(f)}$-VCO signal for output voltage, $U_{0(dig)}$-contets of counter (average output voltage); *cl*-flip- flop clock signal; δ– PWM-triggering pulse.

$$U_0 = \frac{1}{T_s}\int_{t_0}^{t_1} u_0(t)dt = \frac{K_2}{T_s}\int_{t_0}^{t_2} f_u(t)dt \quad (12)$$

where K_2 is digital scaling factor. Equation (10) is modified by using notations in Fig. (6) as follows:

$$\frac{U_0 T_s}{K_2} = \int_0^x f_u(\tau)d\tau = \Pi_1 x, \quad (13)$$

and at the end of interval T_s inside of FPGA, the average value of the output voltage can be evaluated from (13) as follows:

$$U_0 = \frac{K_1}{T} Z_{(u0)} \quad (14)$$

where $Z_u = \Pi_1 x + \Pi_2 \left(x^2/2\right)$ and represents the state of the counter connected to the VCO dedicated for voltage measurement and must be captured from counter for voltage control purposes at the end of interval T_s.

III. Results and Discussion (Simulation and Experimentation)

A. Simulation

The current-mode control based on the proposed principle has been simulated with the use of the MATLAB-SIMULINK (Fig. 7). The current measurement was performed by using the u/f converter. The elements of Simpowersystem toolbox were used and also the whole measurement principle and controllers based on SIMULINK blocks was developed.

It is prescribed that the switching frequency is f_s = 25 kHz (T_s = 40 μs). The parameters used were: L = 270 μH, C = 100 μF, u_0 = 5 V and u_d = 12 V. Figs. 8 show the transient response when the output voltage was controlled during the load change from 6.8 Ω to 3.4 Ω , and vice-versa. The proposed algorithm was also verified by experiments. The experiment was set-up by the cascade control structure were the necessary current reference was calculated by the voltage controller.

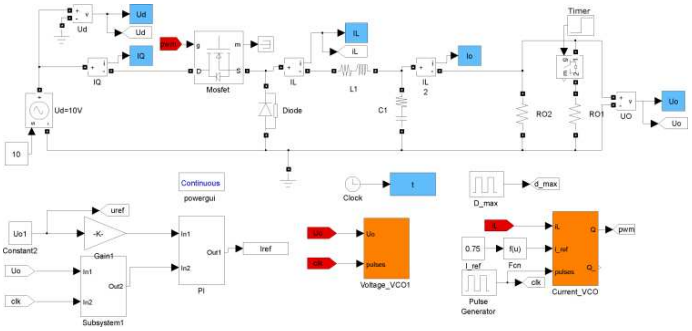

Figure 7. Simulation schema

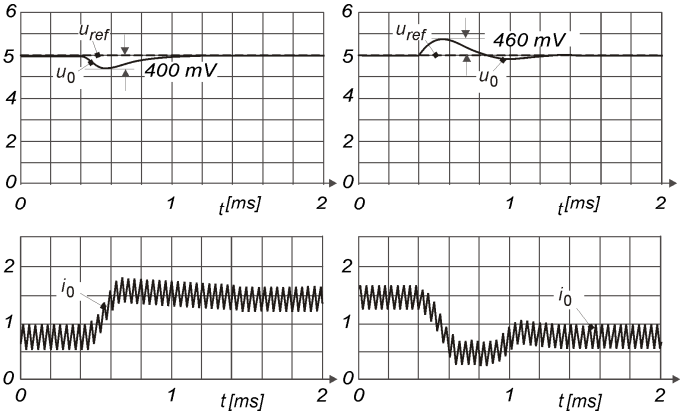

Figure 8. Input and output voltage and current waveforms: reference and output voltage u_{ref} and u_0 respectively (uper diagrams) and inductor current i_L when load changed from 6.8Ω →3.4Ω → 6.8Ω.

For the current and voltage measurements the u/f measurement principle was applied, as was outlined in the previous text. The voltage PI controller parameters were designed frequency domain by using the Bode diagrams. Small signal model based on state space averaging method were used as it is proposed in [6].

B. Experimental set-up

Based on the above described principle of operation the experimental set-up with buck-converter circuit and appropriate FPGA unit was build (Fig. 9). As was claimed in the previous section it was necessary to carry out appropriate processing of the inductor current measured quantity with the aim that the u/f converter will operate in the right area. First of all, u/f converter output frequency starts to vary when its input voltage is greater than 0.7 *V*. When the measured and amplified signal of inductor current has less than ($u_{(iL)}$ < 0.7 V) the u/f converter oscillates with minimum oscillation frequency, whereby the information has been lost, and therefore additional adder circuit was added, which allowed the current measurement from 0 to 2 *A* (0 - 3 *V*). Fig. 10 shows the analogue part of inductor current measurement acquisition system. The current information is provided from shunt resistor and amplified by INA (IC1) circuit. Afterwards the u_{offset} is added to the information of the inductor current.

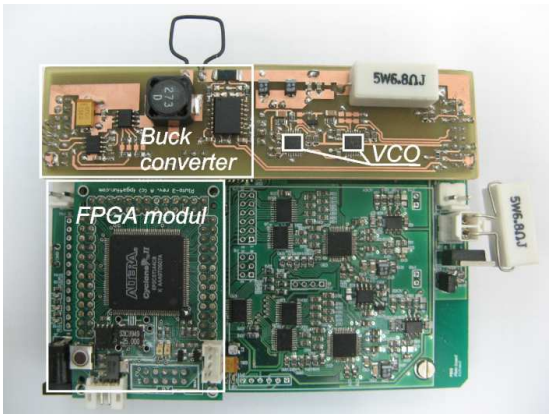

Figure 9. Experimental set-up circuit.

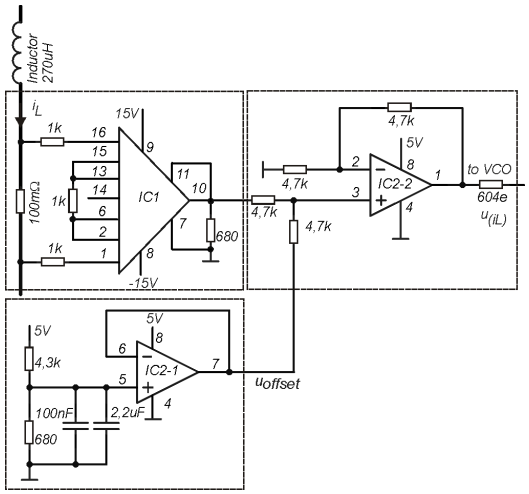

Figure 10. Analogue data aquizition measurement circuit for inductor current.

When the inductor current information is obtained and appropriate processes are connected to the u/f converter (Fig. 11). The whole inductor current measurement "chain" was tested and calibrated as shown in Fig. 12. Yellow area indicates the input voltage range $u_{(iL)} \in (0,\ 3\ V)$. The u/f output frequency changes almost linearly as was presumed in (1). The K_1 digital scaling factor defined in (9) is set as the ratio between the 3V maximum input u/f voltage range and the sum of the two counters. As followed from Fig. 5 for current measurement two counters inside the FPGA were used. The first one counts "the current" during the time period T_{off} and the second one during T_{on}. The meaning of constant K_1 and K_2 should be explained here. From Fig. 12 follows that the maximum frequency of u/f converter

is 140 *MHz*. So between two signals pulses indicated by *cl.* (Fig 3. and Fig. 6) can be counted 5600 (f_{vco}/f_{PWM}) of quanta. Constant K_1 and K_2 can be calculated by:

$$K_1 = K_2 = \frac{f_{pwm}}{f_{vco}} = \frac{1}{5600} \tag{15}$$

The voltage measurement was performed on the same way. Only one digital counter was used inside the FPGA because of almost completely flat voltage waveform.

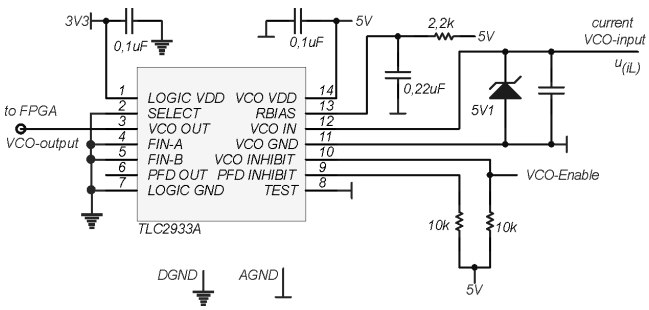

Figure 11. The schema of voltage to frequncy converter for inductor current measurement.

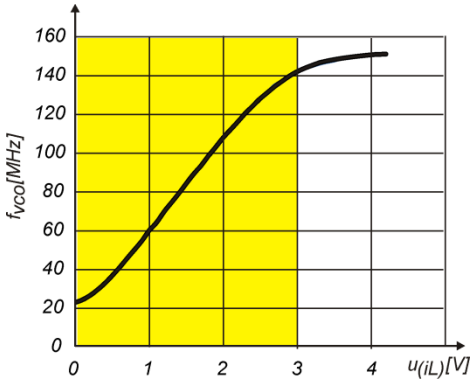

Figure 12. The static characteristic of VCO.

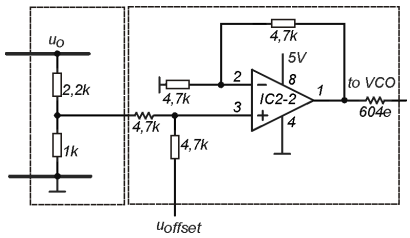

Figure 13. Analogue data aquizition measurement circuit for buck-converter output voltage.

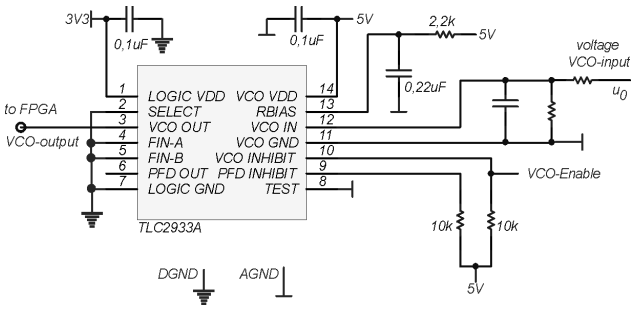

Figure 14. The schema of voltage to frequncy converter for output voltage measurement

This counter is synchronized with the end of triggering pulse δ. The analogue acquisition part of voltage measurement circuit is shown in Fig. 13 and u/f schema is shown in Fig. 13 and VCO circuit in Fig. 14.

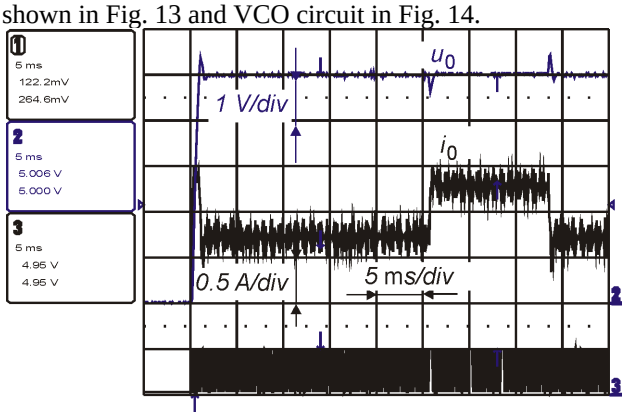

Figure 15. The voltage and current waveform when load was changed from 6,8Ω → 3.4Ω → 6.8Ω

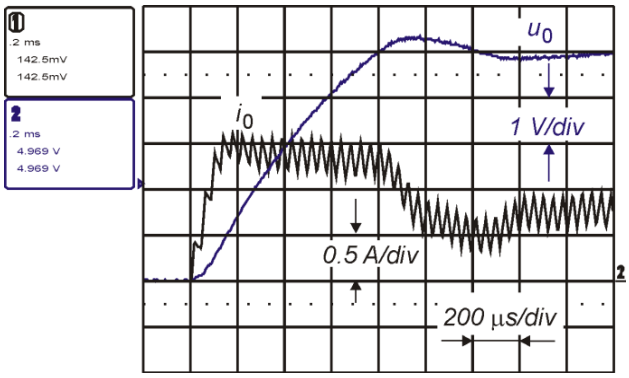

Figure 16. The voltage and current waveform cut-off; start-up voltage and current wave-form

C. *Results and discussion*

The current-mode control based on the proposed principle has been verified by experimentation. The current measurement was performed by using the u/f converter. The switching frequency is set to f_s = 25 *kHz* (T_s= 40 µs) and the buck converter circuit parameters are chosen as was suggested in the simulation: *L*= 270 µ*H*, C = 100 µ*F*, u_0 = 5 *V* and u_d = 12 *V*. The experiment was set-up by the cascade control structure were the necessary current reference was calculated by the voltage controller. For the current and voltage measurements the u/f measurement principle was applied, as was outlined in the previous text. Fig. 15 shows the transient response when load was changed as indicated in the figure capture. The voltage reference was set to *5* V. Fig. 16 shows start-up response of buck-converter output voltage and inductor current. The average inductor current is limited to *1.5* A. Figs. 17 and 18 show close-up when the load has changed from 6,8 Ω → 3.4 Ω. and 3.4 Ω → 6.8 Ω respectively. The voltage controller generates the current reference which changes from 0.75 *A* to 1.5 *A* and vice-versa. The voltage dynamic error was approximately ±400 *mV*.

IV. CONCLUSION

The voltage and current control-mode control algorithm can be performed in a digital way as it is shown in this paper. The VCO based current and voltage measurements enable such approach.

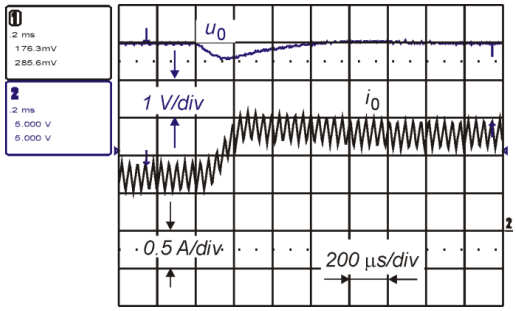

Figure 17. The voltage and current waveform cut-off; when load was changed from 6,8 Ω → 3,4 Ω.

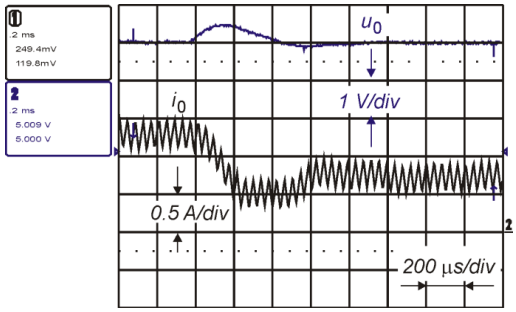

Figure 18. The voltage and current waveform cut-off; when load was changed from 3.4 Ω → 6.8 Ω.

The algorithm is based on average current and voltage measurement by using the voltage to frequency conversion instead of conventional A/D converters. Both measurements were performed by using the VCO. Such an approach is suitable for the implementation of all algorithms in the FPGA circuit. It is, therefore, adequate for many industrial applications such as high power multi-phase DC-DC converters.

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